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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,764	03/03/2004	Norikatsu Takaura	NIT-416	5129

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,764	TAKAURA ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *6-9,16 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) *18* is/are allowed.

6)☒ Claim(s) *1-5 and 10-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/03/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 07/23/2004 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Species I, claims 1-5, 10-15, and 18, in the reply filed on 07/08/2005 is acknowledged.

3. In the Restriction Requirement Paper mailed 06/09/2005, the examiner identified claims 1-5 and 18 as being generic. However, only claims 1 and 5 are generic as nonelected claims 6-9 and 16-17 depend on and comprise all limitations of claims 1 and 5.

4. Claims 6-9 and 16-17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 07/08/2005, as noted above.

Drawings

5. Figure 48 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR

1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "connected in common to the other of the source and the drain" in "the second electrode layer deposited on the phase change material layer of the stacked layer films, serving as bit lines, and being configured so as to be connected in common to the other of the source and the drain, in at least two of the memory cells" of **claim 18** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

7. The claims are objected to because of the following informalities: The auto-spacing feature of the word processor that generates the claims does not appear to function properly. Examples are: claim 1, line 5: "resistorelement"; claim 2, page 50, line 25, "secondelectrode"; and claim 18, page 55, line 21, "depositedin".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. **Claims 1 and 3-5** are rejected under 35 U.S.C. 102(e) as being anticipated by Horii U.S. Patent Application Publication 20030209746 (the '746 reference).

The '746 reference discloses in Figures 3-7, particularly Fig. 7, and respective portions of the specification a semiconductor integrated circuit device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor integrated circuit device having a plurality of memory cells formed on a semiconductor substrate (51), each made up by electrically connecting a resistor element (generally defined by 69/71/91, Fig. 7) in series with a field effect transistor (generally defined by 55/57s/57d);

the resistor element comprising stacked layer films formed of a first electrode layer (69), a phase change material layer (71, paragraph [0019]) made of one phase change material layer - meeting the limitation of one phase change material layer or plural phase change material layers - with resistance values changing by heating treatments (paragraph [0023]), and a second electrode layer (81/83), deposited in that order, and connected to a power source terminal (such as 63 or 83) common to the respective field effect transistors in at least two of the memory cells.

Referring to **claim 3** and using the same reference characters and citations as detailed above for claim 1 where applicable, the reference discloses a semiconductor integrated circuit device comprising a plurality of memory cells formed on a semiconductor substrate, each made up by electrically connecting a resistor element in series with a field effect transistor;

the field effect transistor having either of a source and a drain, connected to a conductive film serving as bit lines (63) of the memory cells, respectively, and the other of the source and the drain, connected to the resistor element;

the resistor element comprising stacked layer films made up of a first electrode layer, a phase change material layer made of one phase change material layer or plural phase change material layers with resistance values changing by heating treatments, and a second electrode layer, deposited in that order, and formed on the conductive film (63) through the intermediary

of an insulation film (such as 65) so as to be individually connected to the respective field effect transistors in the memory cells.

Referring to **claim 4** and using the same reference characters and citations as detailed above for claim 1 where applicable, the reference discloses a semiconductor integrated circuit device comprising a plurality of memory cells formed on a semiconductor substrate, each made up by electrically connecting a resistor element in series with a field effect transistor;

the field effect transistor having either of a source and a drain, connected to a conductive film serving as bit lines (63) of the memory cells, respectively, and the other of the source and the drain, connected to the resistor element;

the resistor element comprising stacked layer films made up of a first electrode layer, a phase change material layer made of one phase change material layer or plural phase change material layers with resistance values changing by heating treatments, and a second electrode layer, deposited in that order, formed on the conductive film (63) through the intermediary of an insulation film (such as 65) and configured such that the first electrode layer and the phase change material layer are divided by the memory cell and the second electrode layer is connected to a power source terminal (83) common to the respective field effect transistors in at least two of the memory cells.

Referring to **claim 5**, the reference further discloses that either of a source and a drain, in the field effect transistor, is connected to the first electrode layer with a plug layer (61s and/or 67) made up by filling up a contact hole (such as 67a), formed in an insulation film, with a conductive material (paragraph [0019]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claim 2** is rejected under 35 U.S.C. §103(a) as being unpatentable over Horii U.S. Patent Application Publication 20030209746 (the '746 reference) in view of Kuge U.S. Patent 6,597,031.

Referring to **claim 2**, the '746 reference discloses a semiconductor integrated circuit device having a plurality of memory cells substantially as claimed and as detailed above for claim 3 but fails to discloses the limitation "to be connected in common" in "the resistor element comprising stacked layer films made up of a first electrode layer, a phase change material layer made of one phase change material layer or plural phase change material layers with resistance values changing by heating treatments, and a second electrode layer, deposited in that order, and being formed on the conductive film through the intermediary of an insulation film so as to be connected in common to the other of the source and the drain, in at least two of the memory cells". Instead, the reference discloses, as detailed above for claim 3, "to be individually connected".

Kuge, in also disclosing a semiconductor integrated circuit device having a plurality of memory cells, teaches in Figs. 1-2 and column 2, lines 5-67, that the stacked resistor elements (generally defined by 31a,b,c and 10a) to be connected in common may result in high integration.

Therefore, it would have been obvious to form the '746 reference's device such that the stacked resistor elements to be connected in common. One would have been motivated to make such a change in view of the teachings in Kuge that such a change may result in high integration.

10. **Claims 10-15** are rejected under 35 U.S.C. §103(a) as being unpatentable over Horii U.S. Patent Application Publication 20030209746 (the '746 reference) in view of Johnson et al. U.S. Patent Application Publication 20050030800.

Referring to **claim 10**, the '746 reference discloses a semiconductor integrated circuit device having a plurality of memory cells substantially as claimed and as detailed above for claim 1 but fails to discloses that the phase change material layer comprises stacked layer films formed of a first phase change material layer made of a first melting point material, and a second phase change material layer made of a material having a melting point higher than that of the first melting point material layer, deposited in that order, and the first phase change material layer is connected to either of the source and the drain, in the field effect transistor.

Johnson, in also disclosing a semiconductor integrated circuit device having a plurality of memory cells (although only one cell is shown in the figures), each made up by electrically connecting a resistor element (16/22/24/26/20) in series with a selection device that may be a transistor (paragraph [0009]), the resistor element (16/22/24/26/20) comprising stacked layer films made up of a first electrode layer (16), a phase change material layer made of plural phase change material layers (22/24/26) with resistance values changing by heating treatments (page 1, particularly paragraph [0016]), and a second electrode layer (20), deposited in that order, teaches that that addition of the additional phase change material layer (22 or 26), which effectively meets the limitation "the phase change material layer comprises stacked layer films formed of a first phase change material layer (24 or 22) made of a first melting point material, and a second phase change material layer (24 or 26) made of a material having a

melting point higher than that of the first melting point material layer (as only required layer 24 is "active" (paragraph [0011] and the other two optional layers (22 and 26) are not active), deposited in that order" as claimed, promotes strong adhesion, integrity, and improved interfaces of electrode to phase change elements (paragraph [0014]).

Therefore, it would have been obvious to form the '746 reference's device such that the phase change material layer (71) comprises stacked layer films formed of a first phase change material layer (24 or 22) made of a first melting point material, and a second phase change material layer (24 or 26) made of a material having a melting point higher than that of the first melting point material layer. One would have been motivated to make such a change in view of the teachings in Johnson that such a change promotes strong adhesion, integrity, and improved interfaces of electrode to phase change elements.

Referring to **claim 11**, the '746 reference further teaches that the first phase change material layer 71 is in a crystallized state (paragraph [0023]) in a state.

Referring to **claim 12**, the '746 reference further teaches, in view of Johnson, that the second phase change material layer 71 is in an amorphous state (paragraph [0023]) in a state.

Referring to **claim 13**, the '746 reference further teaches, in view of Johnson, that the phase change material layer comprises stacked layer films formed of the first phase change material layer (71) in a crystallized state (the '746 reference, paragraph [0023]), and a second phase change material layer (26) in an amorphous state (Johnson, paragraph [0012], and note that since Johnson teaches that layer 26 may be crystalline, layer 26 may also be amorphous),

deposited in that order, and that the first phase change material layer (71) is connected to either of the source and the drain, in the field effect transistor.

Referring to **claim 14**, the '746 reference further teaches, in view of Johnson, that the phase change material layer comprises stacked layer films formed of the first phase change material layer (71) in an amorphous state (the '746 reference, paragraph [0023]), and a second phase change material layer (26) in a crystallized state (Johnson, (paragraph [0012], and note that in a device claim, as far as patentability is concerned, a crystallized state and a crystalline sate is equivalent), deposited in that order, and that the first phase change material layer (71) is connected to either of the source and the drain, in the field effect transistor.

Referring to **claim 15**, the '746 reference further teaches, in view of Johnson, that the phase change material layer comprises stacked layer films formed of the first phase change material layer (71) in an amorphous state (the '746 reference, paragraph [0023]), and a second phase change material layer (26) in a crystallized state (Johnson, (paragraph [0012], and note that in a device claim, as far as patentability is concerned, a crystallized state and a crystalline sate is equivalent), deposited in that order, and that the first phase change material layer (71) is connected to either of the source and the drain, in the field effect transistor, with a plug layer (67, the '746 reference, Fig. 7) formed in a insulation film (65), having an area where a portion of the first phase change material layer is crystallized due to Joule heat generated by flow of current to the plug layer (the '746 reference, paragraph [0023]).

11. **Claim 2** is rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson et al. U.S. Patent Application Publication 20050030800 (the '800 reference) in view of Horii U.S. Patent Application Publication 20030209746 (the '746 reference).

The '800 reference discloses a semiconductor integrated circuit device having a plurality of phase-change memory cells (Fig. 2, where only one cell is shown, paragraph [0026]) where the depicted cell appears "to be connected in common" (as layers 22/24/28 are part of the depicted typical memory cell, and as these layers appear to extend beyond the cell (as generally defined by bottom electrode 16 and selection device 14), the depicted cell and the cells that adjacent to the depicted cell appear to be connected in common), thus meeting the limitation "the resistor element comprising stacked layer films made up of a first electrode layer, a phase change material layer made of one phase change material layer or plural phase change material layers with resistance values changing by heating treatments, and a second electrode layer, deposited in that order, and being formed on the conductive film through the intermediary of an insulation film so as to be connected in common to the other of the source and the drain, in at least two of the memory cells".

However, the '800 reference fails to disclose details of the selection device and thus further fails to disclose other pertinent required elements for the memory device to function such as a power source and a bit line as recited in claims 1 and 2.

The '746 reference, in also disclosing a semiconductor integrated circuit device having a plurality of memory cells as detailed above, teaches all other limitations.

Therefore, it would have been obvious to form the '800 reference's device such that it includes the details taught by the '746 reference. One would have been motivated to make such a change in view of the teachings in the '746 reference that such details made the device a working device, at the time the invention was made.

Allowable Subject Matter

12. Claim 18, in so far as in compliance with the drawing objection detailed above, is allowable over the prior art of record.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor integrated circuit device having a plurality of phase-change memory cells as recited in claim 18, characterized in that the second electrode layer deposited on the phase change material layer of the stacked layer films, serves as bit lines, and is configured so as to be connected in common to the other of the source and the drain, in at least two of the memory cells.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
July 20, 2005